

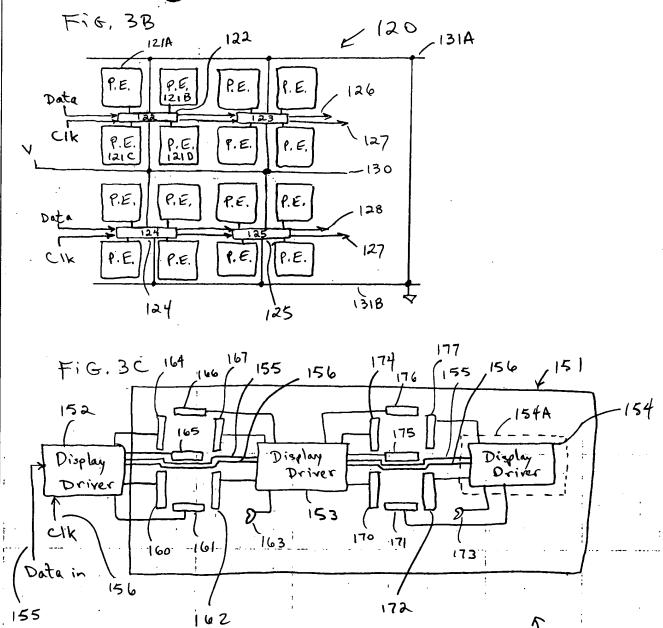
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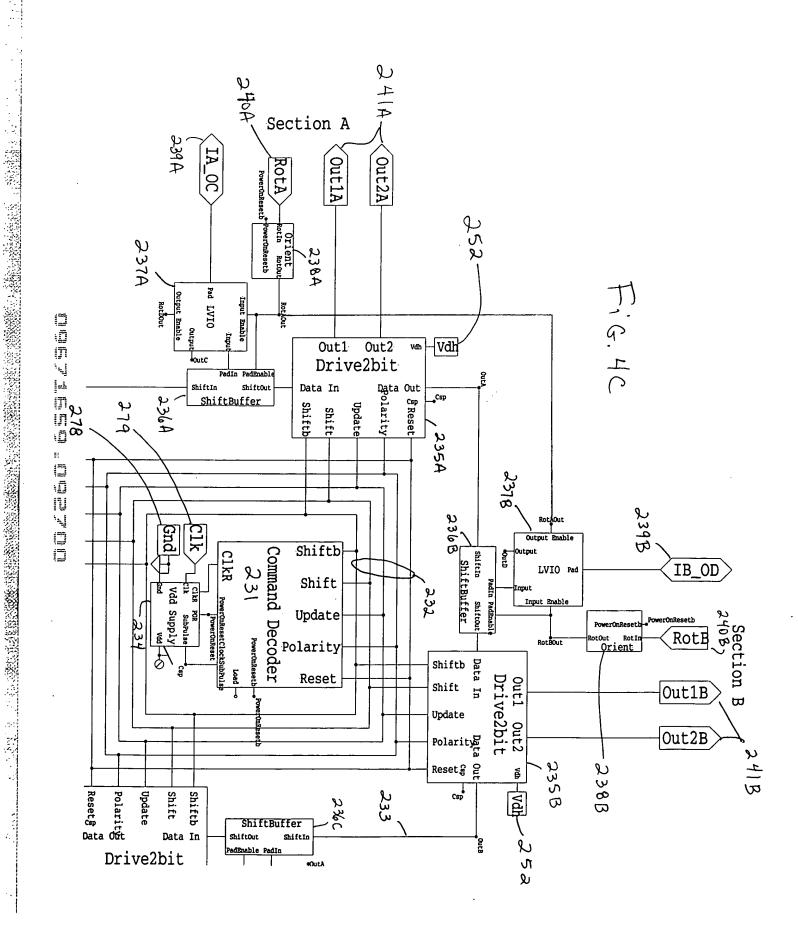
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13-782 42-381 42-383 42-392 42-399 Made in U.

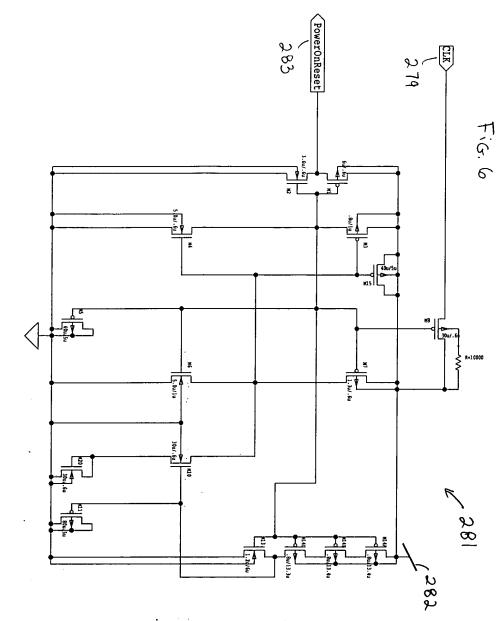


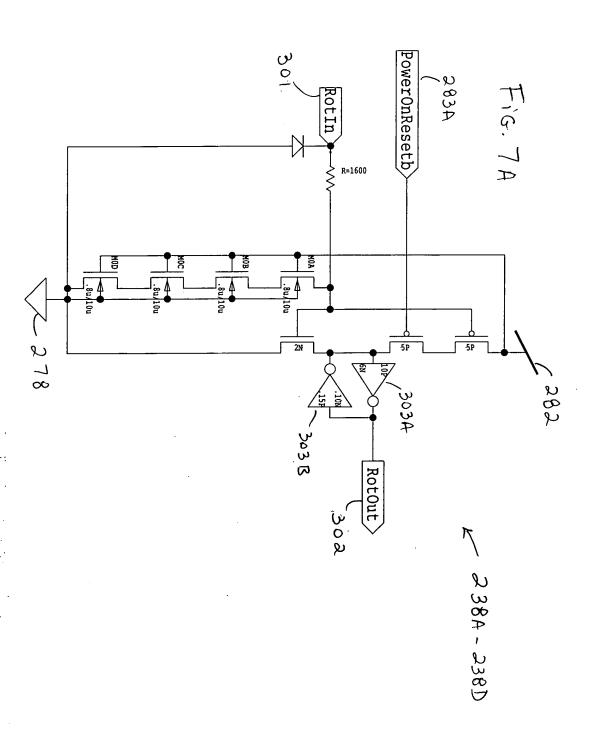
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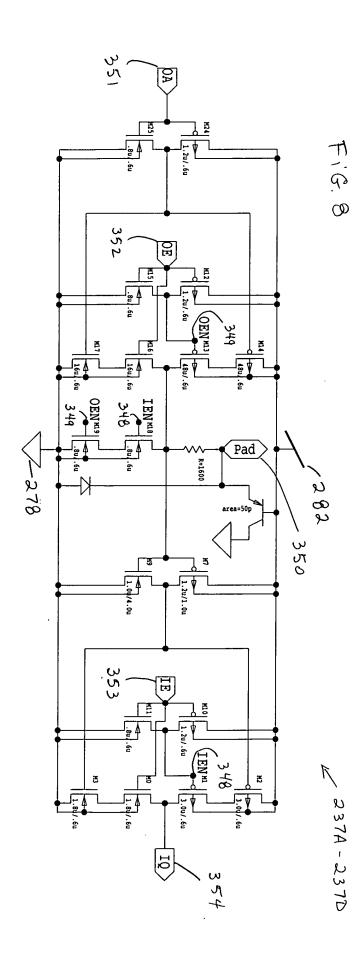
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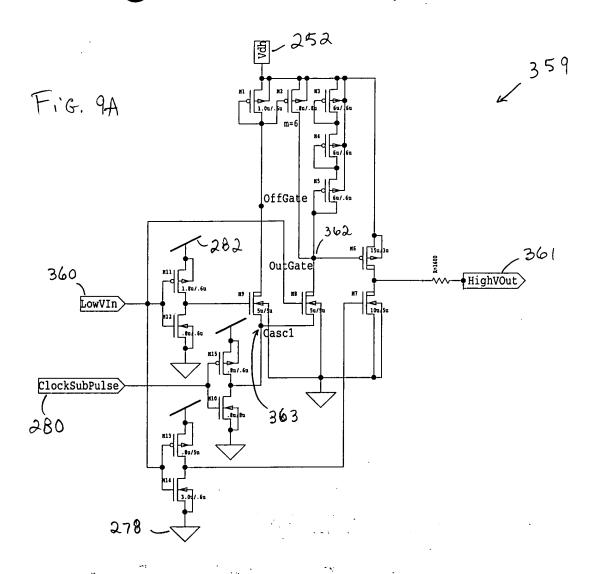


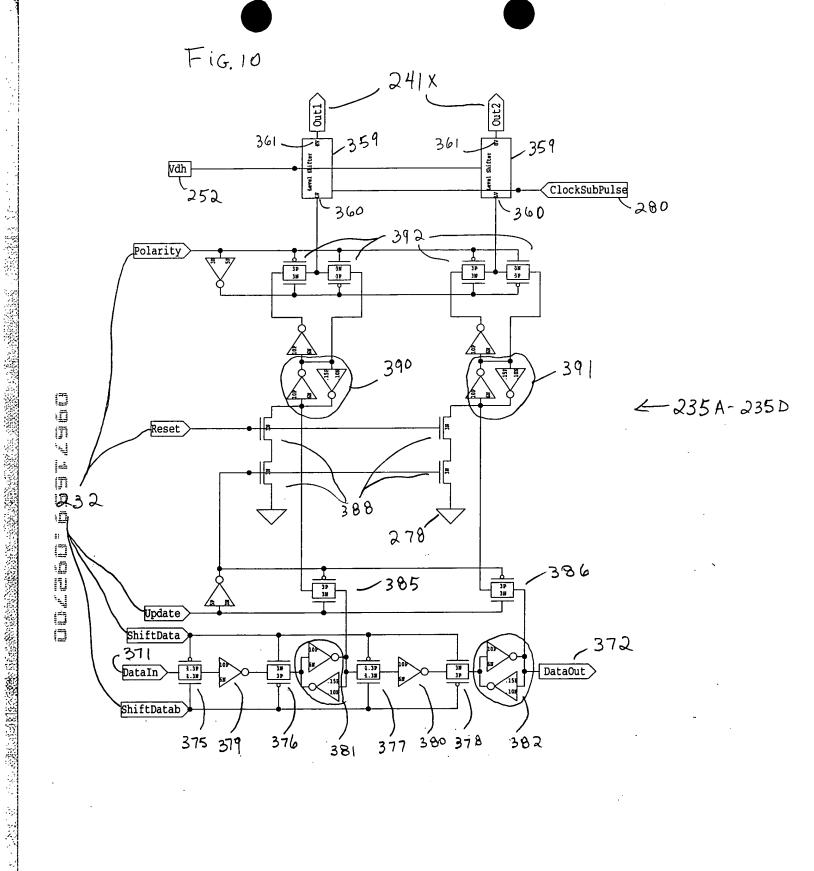
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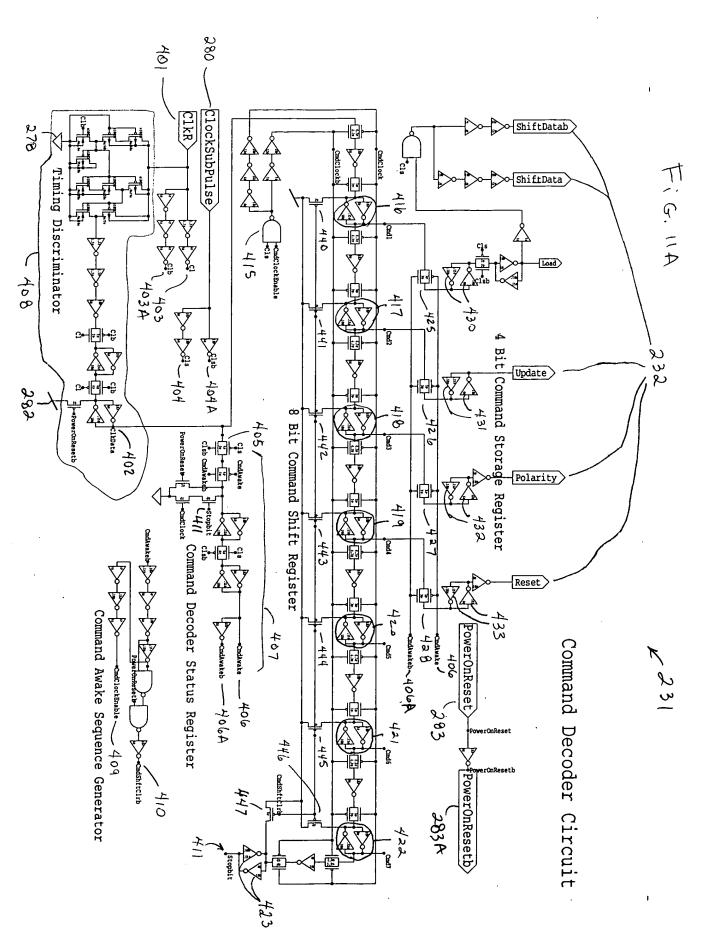




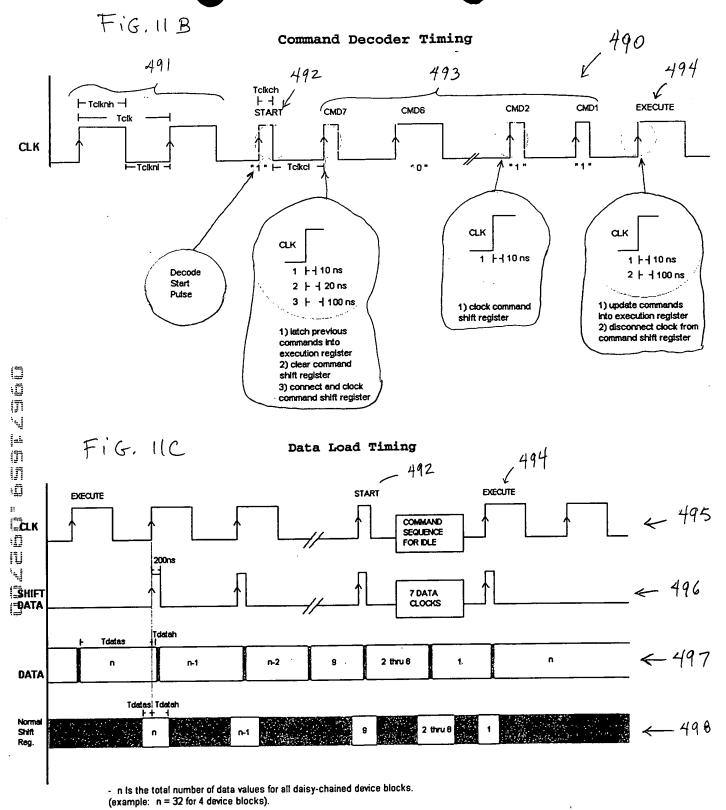








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- data must be low upon start-up and through the first command sequence.

Fig. 11D

liming Discriminator determines that it has received a short clock pulse and cikbata goes "high" (="1") indicating header bit of command/instruction has been received

501

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CondAwake signel goes high after Clk Data goes high and command Storage Register (formed by inverter pairs 430, 431, 432 + 433) is disconnected from Command Shift Register (formed by inverter pairs 416-423)

in command Shift Register, Old instruction data is cleared to low ("o") with assertion of Cmdshft Clrb (when CondShft Clrb goes low! ("O"), and Cond Clock Enable is giver ated/asserted and this allows the clock signal named conditions to Shift Register be provided through commend

Every clock cycle thereafter (until header 1 bit reachs inverter pair 423) shifts instruction bits through the Command shift Legister (short which cycle = high ("1") and long clock sycle = low ("0")

When header bit reaches last stage (inverter pair 423) Stop bit signal is asserted, which stops the shifting (cond clock Enable is deasserted), and Conditione goes low causing the Command Shift register to update the command storage Register

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Power up reset occurs -- default state loads/shifts display data into display drivers which include shift register storage elements 520

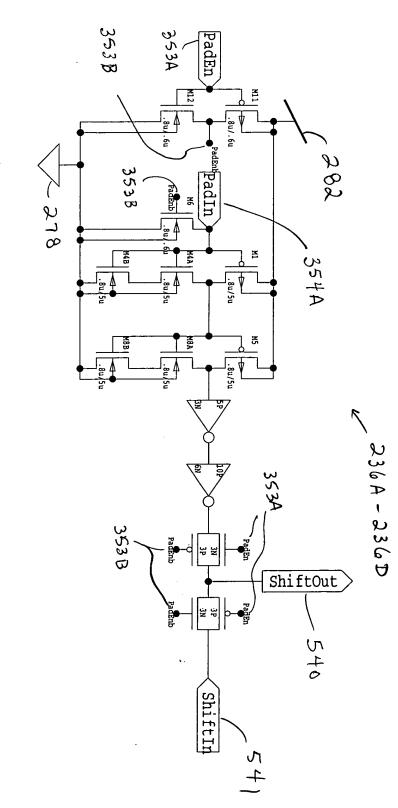
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522

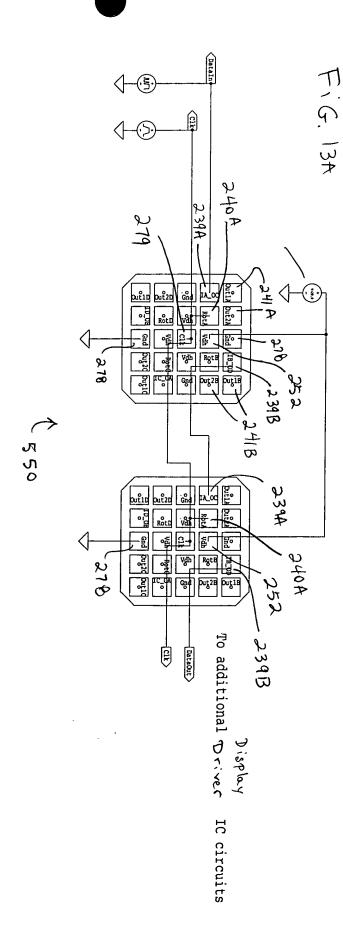
Data shifted in is displayed (may be displayed as data is being shifted in or after all data has been shifted in)

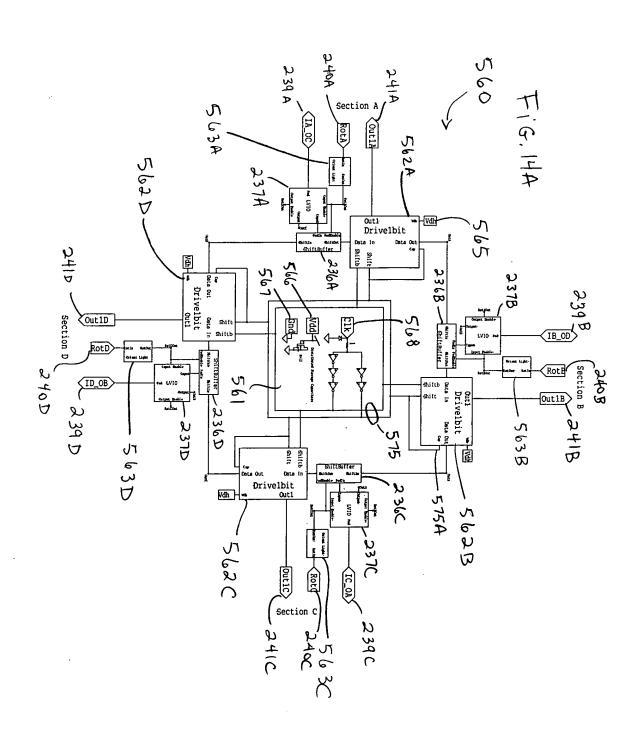
manipulate/control display
with commands to decoders
in display drivers
leig. reset display [clears screen];
or change polarity [eig. for
nematic liquid crystal display
material]; or

set update to low to load
new data and then set
update to high to display
new data

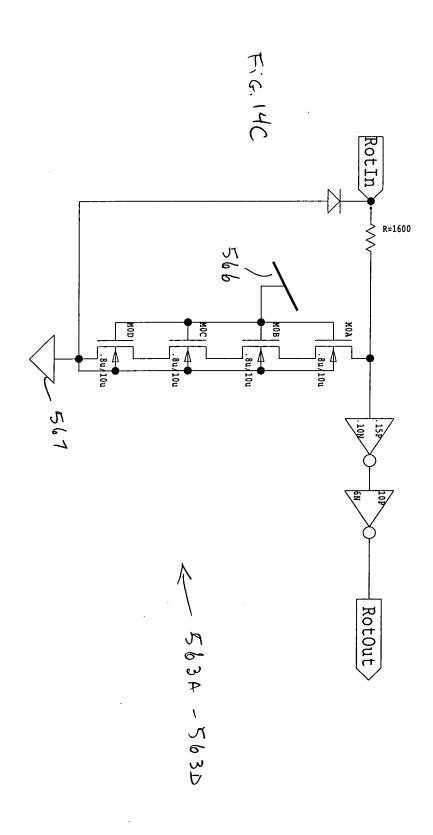


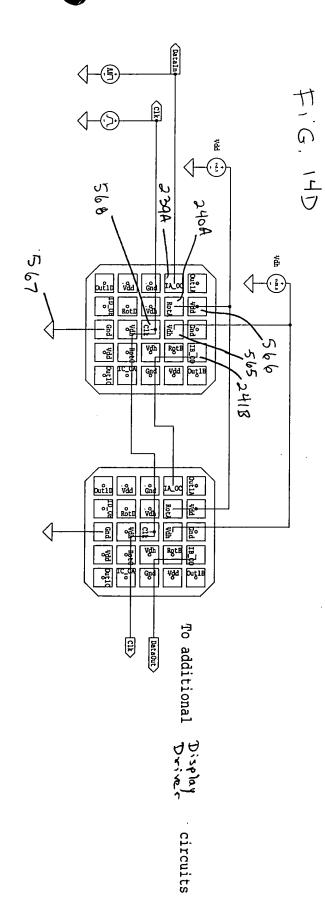
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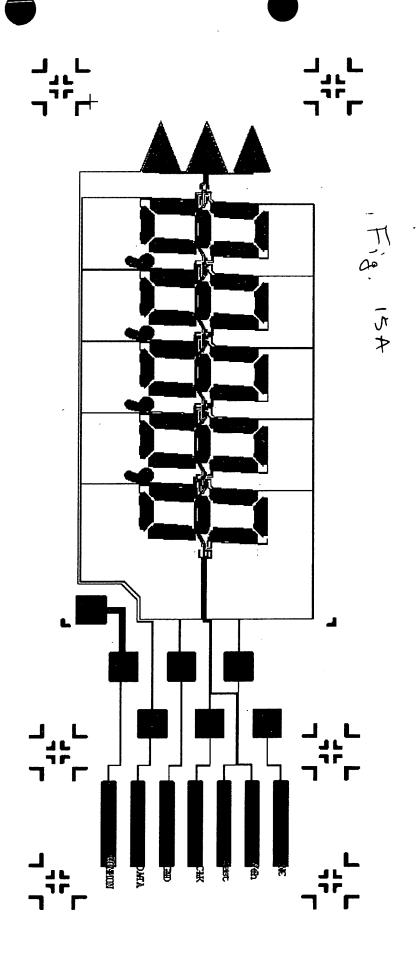




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